

This listing of claims will replace all prior versions, and listing, of claims in the application:

**Listing of Claims:**

1-7. (Canceled)

8. (Previously Presented) A thin film transistor array panel comprising:  
a gate conductive layer formed on an insulating substrate;  
a gate insulating layer on the gate conductive layer;  
a semiconductor layer on the gate insulating layer;  
a data conductive layer formed at least in part on the semiconductor layer and comprising a source electrode and a drain electrode separated from each other;  
a passivation layer formed on the data conductive layer; and  
an IZO conductive layer formed on the passivation layer,  
wherein at least one of the gate conductive layer and the data conductive layer includes a dry-etchable lower film and an upper film formed on the lower film, the upper film including Al or Al alloy and having edges located on the lower film,  
the IZO conductive layer contacts the lower film and a top surface of the upper film, and  
the semiconductor layer has substantially the same planar shape as the data conductive layer except for a portion located between the source electrode and the drain electrode.

9. (Original) The thin film transistor array panel of claim 8, wherein edges of the lower film are located near edges of the upper film adjacent thereto.

10. (Original) The thin film transistor array panel of claim 8, wherein the IZO conductive layer contacts an edge of the lower film.

11. (Canceled).

12. (Original) The thin film transistor array panel of claim 8, wherein the distance between edges of the lower film and edges of the upper film adjacent thereto is substantially uniform.

13. (Original) The thin film transistor array panel of claim 8, wherein the lower film comprises Cr.

14. (Original) The thin film transistor array panel of claim 13, wherein the lower film has a thickness equal to or less than about 500 Å.

15. (Previously Presented) The thin film transistor array panel of claim 8, wherein the IZO conductive layer comprises a pixel electrode contacting the drain electrode, a gate contact assistant contacting a portion of the gate conductive layer, and a data contact assistant contacting a portion of the data line.

16-39. (Canceled)

40. (Previously Presented) The thin film transistor array panel of claim 8, wherein the edges of the upper film include at least opposing edges defining the upper film in a longitudinal direction.

41. (Previously Presented) The thin film transistor array panel of claim 8, wherein the edges of the upper film include at least opposing edges defining the upper film in a transverse direction.

42. (Previously Presented) The thin film transistor array panel of claim 8, wherein the edges of the upper film include all edges defining the upper film.

43. (Previously Presented) The thin film transistor array panel of claim 8, wherein the semiconductor layer has substantially the same planar shape as the lower film of the data conductive layer except for a portion located between the lower film of the source electrode and the lower film of the drain electrode.

44. (Previously Presented) The thin film transistor array panel of claim 43, further comprising an ohmic contact layer interposed between the semiconductor layer and the lower film of the source electrode and the lower film of the drain electrode and having substantially the same planar shape as the semiconductor layer.